**Assignment 10**

**Assignment** All assignments are to be submitted strictly before start of next lab session through online only. Late assignments will not be entertained and will be awarded ‘0’ marks.

1. Below is the code for counter which counts first 5 values mod-3 values. Write the testbench for the same and show the proper output waveforms and understand the code.

*module countseq (input clk, rst, output reg [2:0] modfive, output [1:0] cnt);*

*wire s1;*

*wire [2:0] b1, b2;*

*wire [1:0] b3, b4;*

*assign s1 = (modfive ==5);*

*assign b1 = modfive +1;*

*assign b2 = s1 ? 1 : b1;*

*always @ ( posedge clk, posedge rst) begin*

*if (rst)*

*modfive <= 1;*

*else modfive <= b2;*

*end*

1. Write Verilog code and testbench for 4 bit ring counter.

<https://www.edaplayground.com/x/JjUk>

**Self-Practice and self-evaluation**

1. Write Verilog code and testbench for 4-bit gray counter.
2. Write Verilog code and testbench for 4 bit down counter.